SENRA Academic Publishers, Burnaby, British Columbia
Vol. 3, No. 3, pp. 975-981, 2009
ISSN: 1715-9997

Canadian Journal of pure&applied sciences

A THEORETICAL STUDY OF THE THRESHOLD VOLTAGE SENSITIVITY TO PROCESS VARIATION IN SYMMETRIC DOUBLE GATE MOS DEVICES

Ajay Kumar Singh
Faculty of Engineering and Technology, Multimedia University
Jalan Ayer Keroh Lama 75450 Melaka, Malaysia

ABSTRACT

In this paper we have studied the threshold voltage sensitivity to process variation like channel length, silicon film thickness (t_{Si}) and gate oxide thickness (t_{OX}) in undoped symmetric Double gate (SDG) metal oxide semiconductor field effect transistors (MOSFETs) after developing an analytical model of threshold voltage (V_{Th}). In the proposed model we have introduced a parameter α to take care of Drain-induced barrier lowering (DIBL) effect and quantum confinement effect in sub micron SDG metal oxide semiconductor (MOS) devices. To verify the validity of our developed model, we have compared the simulation results of threshold voltage model with two-dimensional MINIMOS simulator results and found a close agreement. These analytical expressions for sensitivity are solved numerically and compared with published results. The analytical expressions of the sensitivity strongly depend on the device parameter combinations. The study suggests that the threshold voltage sensitivity to length imposes a serious constrain on the scaling of SDG MOS devices. The V_{Th} sensitivity to t_{OX} is not a serious issue for longer SDG MOS devices whereas in deep sub-micron regime, its effect can not be ignored which put restriction on the choice of the gate oxide thickness value.

Keywords: Poisson's equation, threshold voltage sensitivity, electrostatic potential, symmetrical double gate MOS devices, mobile charge sheet density**.**

INTRODUCTION

As Complementary metal oxide semiconductor (CMOS) transistor size is approaching the limit imposed by oxide tunneling and voltage non-scaling as discussed by Assad *et al*. (2000), Jurczak *et al*. (2005) and Ishimaru (2008), double gate (DG) MOSFET is becoming a subject of intense VLSI research because of its good control over short channel effects as suggested by Liang and Taur (2004), Reyboz *et al*. (2006), He *et al*. (2007) and Tsormpatzoglou *et al*. (2007). Double gate structure has been the subject of intensive research due to its ideal 60mV/decade subthreshold slope as shown by Jung and Dimitrijev (2006), scaling by silicon film thickness without high doping, and adjusting threshold voltage by gate work functions. The key factors that limit the scaling of DG MOSFETs are threshold voltage roll-off and drain induced barrier lowering (DIBL). The threshold voltage roll-off has been studied extensively by Chen *et al*. (2003), Reyboz *et al*. (2006), Lu and Taur (2006), Ananthan and Roy (2006), Hamid *et al*. (2007), Lime *et al*. (2008), Tsormpatzoglou *et al*. (2008) and Gong *et al*. (2008).

The threshold voltage of DG MOSFETs is a strong function of gate length (L) and silicon film thickness (t_{Si}). An interesting application of the analytical threshold voltage (V_{Th}) model is to study threshold voltage (V_{Th}) sensitivity quantitatively in a more thorough and easier way than the numerical solutions to see the effect of the process variations. Cerderia *et al*. (2008) has performed simulation based study to see V_{Th} sensitivities to L and t_{Si} but they focused only on a single technology node. In this paper authors neither have given any attention on the impact of t_{OX} on V_{Th} variation nor provided a quantitative and systematic analysis. Chen *et al*. (2003) have studied the V_{Th} sensitivities to process parameters in different way and provided the useful information about the scaling limit of DG MOSFETs but their model is lack of DIBL effect. Their model also overestimates the threshold voltage sensitivity parameter to length for thin silicon film.

In the present paper, we have derived the analytical expression for the electrostatic potential in the symmetric double gate (SDG) MOSFETs by solving Poisson's equation under appropriate boundary conditions. The electrostatic potential along the film thickness reduces with increase in film doping concentration as well as source/drain concentration. We have included the DIBL effect and quantum confinement effects in our model and verified the developed model with a close agreement with two-dimensional MINIMOS Simulator results. The analytical models of V_{Th} sensitivities to process variations show a strong dependence on the device parameter combinations. The numerical value of threshold voltage

*Corresponding author email: ajay.singh@mmu.edu.my

sensitivity parameter to length is very close to reported result (~6.8mV/nm) by Takeuchi *et al*. (2001) for very thin silicon film.

Mathematical Formulation

Figure 1 shows the schematic diagram of an undoped symmetric double gate MOSFET (SDG). The channel electrostatic potential under threshold condition is governed by the Poisson's equation with only the inversion charge term included

$$\frac{\partial^2\psi}{\partial x^2} + \frac{\partial^2\psi}{\partial y^2} = \frac{q}{\varepsilon_{si}} n_i e^{\frac{q}{KT}(\psi - \psi_F)} \quad (1)$$

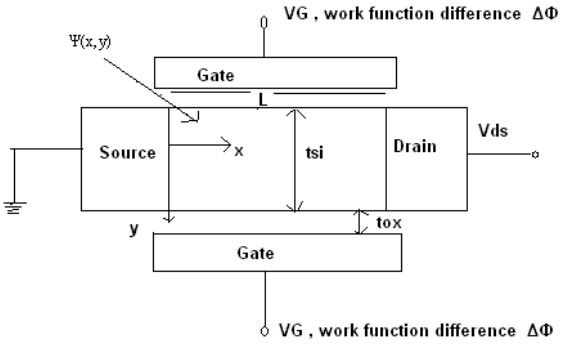

Fig. 1. Schematic diagram of a Symmetric DG MOSFET.

Where Ψ is the electrostatic potential with respect to Fermi level in the source, n_i is the intrinsic electron density and Ψ_F is the non equilibrium quasi-Fermi level with respect to Fermi level in the source and satisfying following boundary conditions; $\Psi_F(0,y)=0$ and $\Psi_F(L,y)=V_{ds}$. According to these two boundary conditions, Ψ_F incurs most of its change near the drain end and stays close to zero in the mid-channel and near source regions. CGA assumes that the Quasi-Fermi potential Ψ_F stays constant along the Y-direction because the current flows along the X-direction i.e. along the channel. Based on these observation $\Psi_F(x,y)$ can be approximated to be zero everywhere except at the end of the channel. Such approximation is implemented by modifying equation (1) as

$$\frac{\partial^2\psi}{\partial x^2} + \frac{\partial^2\psi}{\partial y^2} = \frac{q}{\varepsilon_{si}} n_i e^{\beta\psi} \quad (2)$$

Where β= (q/KT).

In DG MOS, junction depth (X_j) is equal to the silicon body thickness (t_{si}), which is also an important device parameter which is defined by a particular technology. For simplicity of the analysis we have ignored this parameter as well as quantum confinement effect, which dominates for t_{si}<10nm, in the present communication.

Ψ(x,y) in equation (2) can be expressed as

$$\Psi(x,y)=\Psi_0(x)+\Psi_1(x,y) \quad (3)$$

Where $\Psi_0(x)$ is the solution of 1-D Poisson's equation

$$\frac{d^2\psi_0}{dx^2} + \frac{d^2\psi_0}{dy^2} = \frac{q}{\varepsilon_{si}} n_i e^{\beta\psi_0} \quad 4(a)$$

And the solution of equation (4a) is given by Chen *et al*. (2003)

$$\psi_0(x) = \psi_{0m} + \frac{1}{\beta}\ln(\sec^2 B(\frac{x}{L} - \frac{1}{2})) \quad 4(b)$$

Where $\psi_{0m} = V_{bi} - \frac{2}{\beta}\ln\frac{2 + e^{\frac{\beta V_{bi}}{2}}\frac{L}{\lambda_D}}{\pi}$,

represents the minimum potential in the source-channel-drain junction without intervention of the gate bias.

And

$$B = \frac{\pi}{1 + 2e^{\frac{-\beta V_{bi}}{2}}\frac{\lambda_D}{L}}$$

$\lambda_D = \sqrt{\frac{2\varepsilon_{si}}{\beta q n_i}}$ called intrinsic Debye Length

$\Psi_1(x,y)$ is the solution of the remnant 2-D equation

$$\frac{\partial^2\psi_1(x,y)}{\partial x^2} + \frac{\partial^2\psi_1(x,y)}{\partial y^2} = \frac{q}{\varepsilon_{si}} n_i e^{\beta\psi_0}[e^{\beta\psi_1(x,y)} - 1] \quad 4(c)$$

With boundary conditions; $\psi_1(0,y)=0$, $\psi_1(L,y)=0$ and field continuity equation at the interface. We have solved the equation 4(c) by using separation of variable technique and solution is given as,

$$\psi_1(x,y) = [1 + \{1 + 2\ln Sec(\frac{x}{L} - \frac{1}{2}) - \frac{\rho^2 L^2}{2}(\frac{x}{L} - \frac{1}{2})^2 + D\}^{\frac{1}{2}}]\frac{(V_{GS} - \Delta\phi)}{Cosh\rho\gamma} Cosh(\rho y) \quad (5)$$

Where ρ is a separation constant, V_{GS} is gate source voltage, ΔΦ is work function difference of the materials and $D = \frac{\rho^2 L^2}{8} - 2\ln Sec\frac{B}{2}$

After adding equations 4(b) and (5), one can get the potential distribution Ψ(x,y) in the symmetric double gate MOSFET. The minimum electrostatic potential $\Psi_{min}(y)$ (i.e. virtual cathode) in the channel can be found through

$$\frac{\partial \psi(x,y)}{\partial x} = 0 \quad \text{And given as}$$

$$\psi_{\min}(y) = \psi_{0m} + \delta\left(\frac{V_{GS} - \Delta\phi}{Cosh\gamma\rho}\right)Cosh\rho y \qquad 6(a)$$

Where

$$\delta = [1 + \{1 + 2\ln SecB\sqrt{\frac{A(\eta-1)}{2}} - \frac{\rho^2 L^2}{4}A(\eta-1) + D\}^{\frac{1}{2}}]$$

A= (5/2) $(1/B^2)$, $\eta = \sqrt{1 - \frac{4F}{A^2}}$, F=$\frac{15}{2}\frac{1}{B^5}(B-\xi)$

and $\xi = \frac{\rho^2 L^2}{2B}$

The minimum electrostatic potential, along the channel for SDG, occurs at

$$\left(\frac{x_{\min}}{L}\right) = \frac{1}{2} - \sqrt{\frac{A}{2}}\sqrt{\eta - 1} \qquad 6(b)$$

From expression 6(b), it is clear that for η=1, the minimum potential along the channel occurs at the middle of the channel, as in the case of long channel MOS devices. This condition is satisfied,

$$\text{When } \sqrt{1 - \frac{4*F}{A^2}} = 1 \quad \text{or} \quad \frac{4*F}{A^2} = 0 \qquad 6(c)$$

i.e either F=0 or A=∞. A=∞, only when L→0 which is physically not possible.

$$\text{Therefore, F=0 which gives } \rho = \sqrt{2} * \frac{B}{L} \qquad 6(d)$$

To include the DIBL effect in channel potential of the Symmetric Double Gate MOSFET, we have modified the expression 6(d) as

$$\rho = \left(\frac{\alpha B\sqrt{2}}{L} + \frac{V_{ds}}{L}\right) \qquad 6(e)$$

Where, α is a fitting parameter to take care of DIBL effect and expressed in volt. For Vds=0 and α=1, equation 6(e) reduces to ρ=√2 (B/L). Under this condition η=1 and the minimum position will occur at (L/2). As V_{ds} or α increases, the parameter η increases and hence x_{min} moves towards the source end. This is called DIBL effect. The minimum surface potential is obtained by substituting $y=\pm t_{si}$ in equation 6(a) and given as

$$\psi_{s\min} = \psi_{0m} + \delta\left(\frac{V_{GS} - \Delta\phi}{Cosh\gamma\rho}\right)Cosh\left(\frac{t_{si}}{2}\rho\right) \qquad (7)$$

The threshold voltage is that value of gate voltage at which a conducting channel is induced at the surface of the MOSFET. Therefore, the threshold voltage is taken to be that value of gate source voltage for which ψsmin = $2\varphi_f$, where φ_f is difference between the extrinsic Fermi level in the bulk region and intrinsic Fermi level. Thus, substituting $V_{GS}=V_{Th}$ in expression (7) we get;

$$V_{Th} = \Delta\phi + \frac{Cosh\gamma\rho}{Cosh\rho\frac{t_{si}}{2}}\left(\frac{\psi_{s\min} - \psi_{0m}}{\delta}\right) \qquad (8)$$

The equation (8) shows that threshold voltage of undoped symmetric double gate MOSFET dependent on V_{ds} and silicon thickness (t_{si}) whereas the proposed model of Chen *et al.* (2003) is independent of V_{ds}. The threshold voltage dependence on the drain-bias is important for digital applications. The DIBL causes threshold voltage to be a function of the operating voltages. To show the validity of our developed model, we compared the simulation results of equation (8) with MINIMOS simulator and found a close agreement as shown in figure 2.

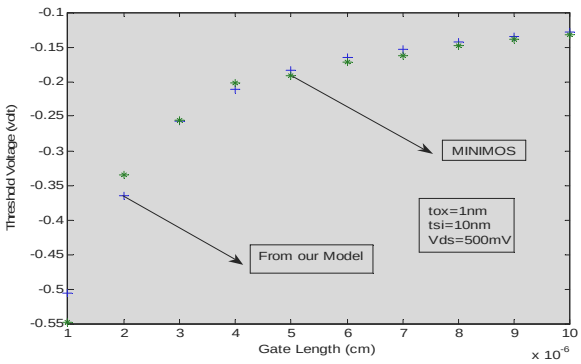

Fig. 2. Comparison of our simulated results with MINIMOS simulator results.

An interesting application of analytical V_{Th} model is to perform quantitative threshold voltage sensitivity analysis of SDG MOSFETS to access the effects of process variation. To demonstrate, V_{Th} sensitivities to process variation, we have derived the analytical models for $(\delta V_{Th}/\delta L)$, $(\delta V_{Th}/\delta t_{OX})$ and $(\delta V_{Th}/\delta t_{Si})$. Using equation (8), the V_{Th} sensitivity to L is given as:

$$\frac{\delta V_{Th}}{\delta L} = \left(\frac{2\phi_B - \psi_{om}}{\delta}\right)\left[\frac{\cosh(\rho\frac{t_{Si}}{2})\gamma\sinh(\gamma\rho) - (\frac{t_{Si}}{2})\cosh(\gamma\rho)\sinh(\rho\frac{t_{Si}}{2})}{\cosh^2(\rho\frac{t_{Si}}{2})}\right]K11$$

$$-\frac{\cosh(\gamma\rho)}{\cosh(\rho\frac{t_{Si}}{2})}\left[\frac{\delta K12 + (2\phi_B - \psi_{om})K13}{\delta^2}\right] \qquad (9)$$

Where

$$K11 = \frac{(L + K\lambda_D)(\frac{-V_{ds} K\lambda_D}{L^2}) - (\pi\sqrt{2} + V_{ds}(1 + K\frac{\lambda_D}{L}))}{(L + K\lambda_D)^2}$$

$$K = 2e^{-\frac{\beta V_{bi}}{2}}, K12 = -(\frac{2}{\beta})\frac{\pi}{(2 + Al\frac{L}{\lambda_D})}(\frac{Al}{\lambda_D}), Al = (\frac{2}{K}), K13 = \frac{d\delta}{dL}$$

Equation (9) shows the dependence of the V_{Th} sensitivity to L on the gate length, silicon film thickness and gate oxide thickness. Our analytical expression clearly shows that as L→0, V_{Th} sensitivity to L approaches to infinity. This reflects that a small change in length causes a large variation in threshold voltage of submicron SDG MOS devices.

Using equation (8) the V_{Th} sensitivity to t_{OX} can be modeled as:

$$\frac{\delta V_{Th}}{\delta t_{OX}} = \frac{m1\rho}{\cosh(\frac{t_{Si}\rho}{2})}\sinh(\gamma\rho) \quad (10)$$

Where $m1 = \frac{(2\phi_B - \psi_{om})}{\delta}$

$$\gamma = (\frac{t_{Si}}{2} + t_{OX})$$

Using $m = \frac{m1}{\cosh(\frac{t_{Si}\rho}{2})}$ and expanding sinh(γρ) by using Taylor's expansion and retaining only first term we get,

$$\frac{\delta V_{Th}}{\delta t_{OX}} = MX + cons\tan t \quad (11)$$

Where $M = m\rho$

And constant=$(M\frac{t_{si}}{2})$ and $X = t_{0x}$

From equation (11) it is clear that the V_{Th} sensitivity to t_{OX} varies linearly with gate oxide thickness for SDG MOS devices of very thin gate with a slope of [$K\rho^2$/cosh ((t_{Si}/2) ρ)]. Therefore, by knowing the slope of the curve, one can also find out the value of the parameter ρ and then α for a given silicon film thickness.

The V_{Th} sensitivity to t_{Si} is

$$\frac{\delta V_{Th}}{\delta t_{Si}} = \frac{-(m1\rho)}{2\cosh^2(\gamma - t_{OX})\rho}[\sinh(t_{OX}\rho)] \quad (12)$$

From relations (9), (10) and (11) it is clear that the analytical models of the threshold voltage sensitivities strongly depend on the device parameter combinations.

The positive and negative signs of the $\frac{\delta V_{Th}}{\delta L}$ and $\frac{\delta V_{Th}}{\delta t_{Si}}$ respectively are dictated by short channel effects (SCEs). From relation (12) it is seen that if ρ→0 i.e. as L→∞ the parameter $\frac{\delta V_{Th}}{\delta t_{Si}} \to 0$. In other words we can say that for very long channel SDG MOS devices the process variation is not a limiting factor.

Expanding the sinh term in equation (12) and retaining only two terms, we have

$$\frac{\delta V_{Th}}{\delta t_{Si}} = \frac{-(m1\rho)}{2\cosh^2(\gamma - t_{OX})\rho}(t_{OX}\rho)[1 + (t_{OX}\rho)^2/6] \quad (13)$$

DISCUSSION

We have compared our model's results with Munteanu *et al*. (2006) model results as shown in figure 3. The two models show a good agreement near the surfaces. The maximum difference of 2% between the two models is reported near the centre due to the negligence of quantum mechanical effect in our proposed model.

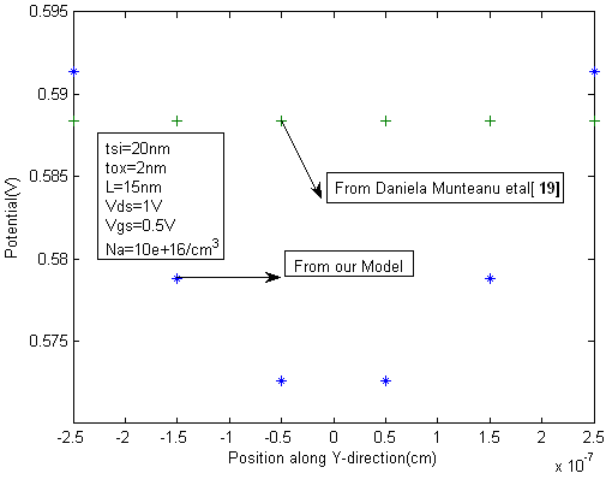

Fig. 3. A comparison of electrostatic potential with two models.

The effect of the silicon film doping on the threshold voltage is less distinct for deep submicron SDG MOS devices as shown in figure 4. It is also observed that threshold voltage takes lower value for any SDG MOS device of lightly doped.

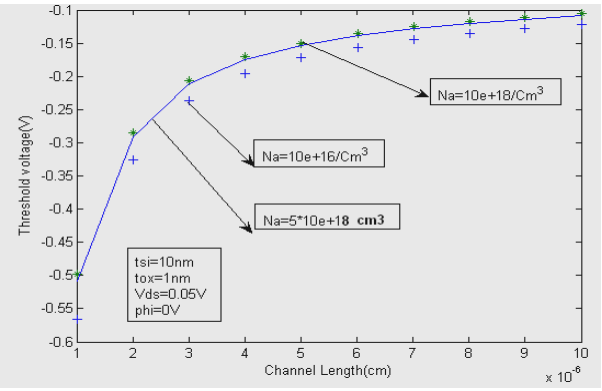

Fig. 4. Variation of threshold voltage with channel length for three different substrate doping concentration.

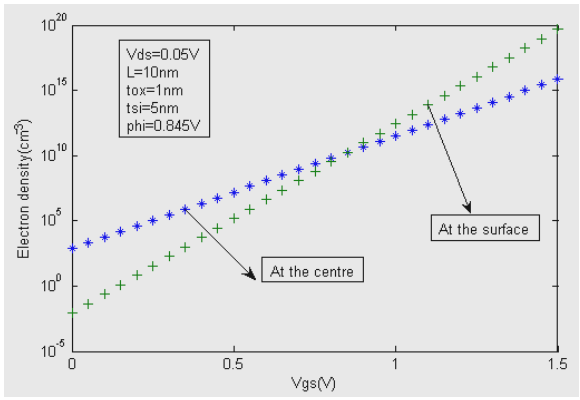

Fig. 5. Variation of electron density with Vgs for surface and Centre.

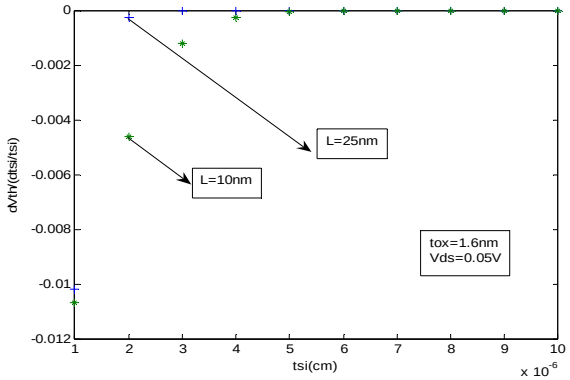

Fig. 6. Variation of threshold voltage sensitivity parameter with silicon film for two channel length.

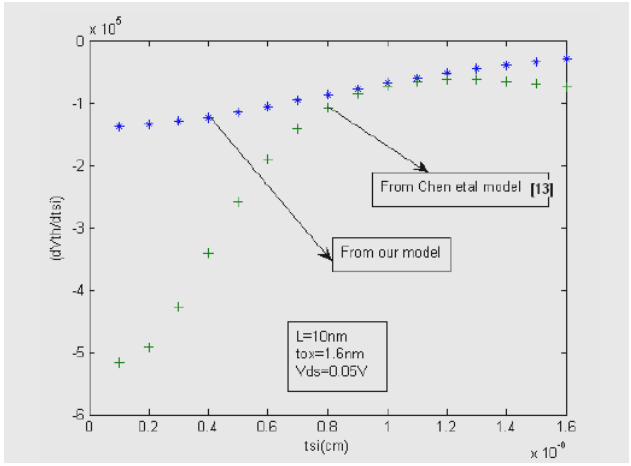

Fig. 7. Threshold voltage sensitivity to tsi parameter with t_{Si}: A comparison.

Figure 5 shows the variation of electron density with gate voltage at the surface and centre. The electron density varies linearly with gate voltage. It is observed that for Vgs<0.9V centre's electron density exceeds the surface electron density whereas for V_{gs}>0.9 V the surface electron density exceeds the centre's electron density and device will enter into the conduction mode. Therefore, we can conclude that there are two distinct regions of operation in the SDG MOS devices, just like in a conventional bulk MOSFETs.

We have plotted the V_{Th} sensitivity to t_{Si} with film thickness for two SDG MOS devices at V_{ds}=0.05V in figure 6. For thicker silicon film (i.e. t_{si}≥40nm), sensitivity parameter remains constant with the thickness irrespective of the channel length. An appreciable change is observed only for t_{si}<40nm. This study clearly shows that threshold voltage variation with silicon film is only a limiting factor for submicron MOS devices and put a stringent requirement for thin silicon film.

We have compared the simulated results of V_{Th} sensitivity to t_{Si} from our model and Chen *et al*. (2003) model as shown in figure 7. These two models show a good agreement for thicker silicon film whereas for thinner film two models deviate very much because of negligence of DIBL effect in Chen *et al*. (2003) model.

In figure 8, we have plotted the results obtained from equations (12) and (13). The two results shows an excellent agreement for thinner film whereas for thicker film (i.e. t_{si}>10nm) both results show disagreement.

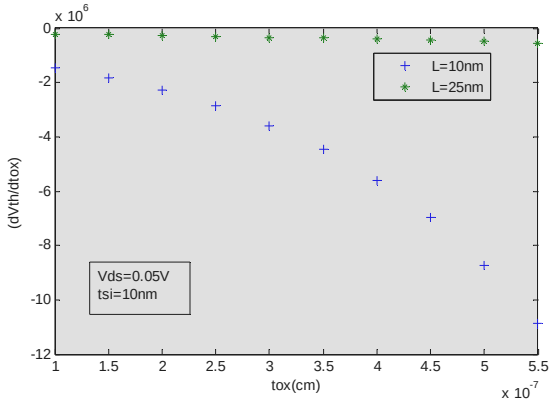

Fig. 9. Variation of threshold voltage sensitivity to tox with gate oxide thickness for two SDG MOS devices.

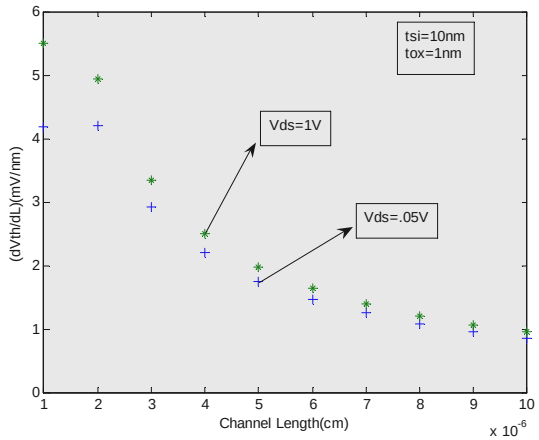

Fig. 10(a). Threshold voltage change versus channel length of SDG MOSFETs for two values of drain voltage.

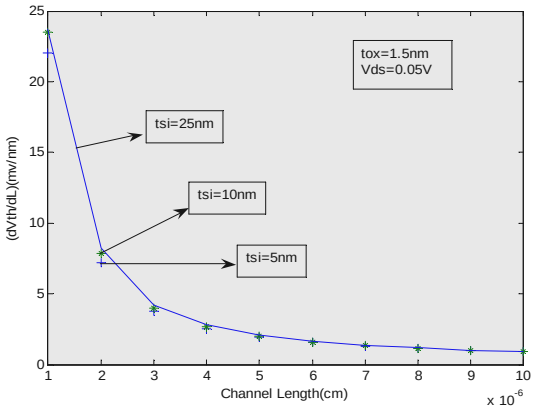

Fig. 10(b). Variation of threshold voltage sensitivity to length with channel length for three different silicon film thicknesses.

The parameter $(\frac{\delta V_{Th}}{\delta t_{OX}})$ is calculated for different values of gate oxide thickness (t_{OX}) by using equation (10) and results are plotted in figure 9. From graph, it is clear that this sensitive parameter shows a slight variation with gate oxide thickness for longer SDG MOS devices after t_{OX}≥2.5nm. An appreciable effect of t_{OX} on $(\frac{\delta V_{Th}}{\delta t_{OX}})$ is observed for sub-micron SDG MOS devices. The sensitive parameter $(\frac{\delta V_{Th}}{\delta t_{OX}})$ falls exponentially with increase in the value of gate oxide thickness. This falls in the parameter put a restriction on the choice of the gate oxide thickness in SDG submicron MOSFETs. This result is contradicting the findings of Chen *et al*. (2003) that the gate oxide thickness causes relatively insignificant threshold voltage variation.

From figure 10(a) it is observed that the sensitivity parameter decreases with channel length irrespective of the value of drain voltage. The sensitivity to L is always higher for higher drain voltage. This result shows that by applying proper drain voltage one can control the change of threshold voltage due to any variation in channel length.

The effect of silicon film thickness (t_{si}) on the threshold voltage (V_{Th}) sensitivity to L is negligible for SDG MOS devices of L≥50nm. The sensitive parameter is only affected by the film thickness for deep submicron MOS devices as shown in figure10 (b). A small V_{Th} sensitivity to L is observed for thinner film thickness. The calculated value of (dV_{Th}/dL) from our model is about 6.3mV/nm for tsi=7nm which is very close to reported result of 6.8mV/nm by Tokeuchi *et al*. (2001) whereas Chen *et al*. (2003) model overestimate this parameter for thinner silicon film. For tighter control over geometric variations, one can use a SDG MOS device of length L≥30nm with thinner silicon film thickness and oxide thickness.

CONCLUSION

In conclusion, the electrostatic potential in SDG MOS devices reduces along the silicon film thickness due to increase in silicon film doping or source/drain concentration. Threshold voltage of the SDG MOS devices can be adjusted at the desired value by choosing proper gate material. For long SDG MOS devices V_{Th} sensitivity to t_{OX} is independent of the gate oxide thickness whereas for submicron SDG MOS devices this parameter can not be ignored. The V_{Th} sensitivity to L decreases exponentially with increase in channel length irrespective of film thickness. The calculated value of the parameter $\frac{\delta V_{Th}}{\delta L}$ is very close to reported result for thin silicon film. The study clearly shows the stringent requirement for thin silicon film.

The limitation of the present study is that the derived model can not be used for a SDG device having film thickness t_{si}<10nm due to non inclusion of quantum mechanical effects.

REFERENCES

Ananthan, Hari. and Roy, Kaushik. 2006. A compact physical model for yield under gate length and body thickness variations in nanoscale double-gate CMOS. IEEE Trans. Electron Devices. 53:2151-2159.

Assad, Farzin., Zhibin, Ren., Vasileska. D., Datta, S. and Lundstorm, M. 2000. On the performance limits for Si MOSFET's: A theoretical study. IEEE Trans on Electron Devices. 47:232-240.

Cerderia, A., Moldovan, O., Iniguez, B. and Estrada, M. 2008. Modeling of potentials and threshold voltage for symmetric doped double-gate MOSFETs. Solid-state Electronics. 52:830-837

Chen, Q., Harrell, M., Evans. and Meindl, DJ. 2003. A Physical short-channel threshold voltage model for undoped symmetric double-gate MOSFETS. IEEE Trans Electron Devices. 50:1631-1637.

Gong, Jing-Feng., Chan, CH., Philip. and Chan, M. 2008. An explicit surface-potential-based model for undoped double-gate MOSFETs. Solid-state Electronics. 52:282-288.

Hamid, Hamdy Abd Ei., Guitart, JR. and Iniguez, B. 2007. Two-dimensional analytical threshold voltage and subthreshold swing models of undoped symmetric Double-gate MOSFETs. IEEE Trans on Electron Devices. 54:1402-1408.

He, Jin., Liu, Feng., Zhang, Jian., Feng, Jie., Hu, Jinhua., Yang, S. and Chan, M. 2007. A Carrier-Based Approach for Compact Modeling of the long-channel undoped Symmetric double-gate MOSFETs. IEEE Trans on Electron Devices. 54:1203-1209.

Ishimaru, K. 2008. 45nm/32nm CMOS –challenge and perspective. Solid-state electronics. 52:1266-1273.

Jung, Hak Kee. and Dimitrijev, S. 2006. Analysis of subthreshold carrier transport for ultimate DGMOSFET. IEEE Trans on Electron Devices. 53:685-691.

Jurczak, Malgorzata., Veloso, Anabela., Rooyackers, Rita., Augendre, Emmanuel., Mertens, Sofie., Rotschild, Aude., Scaekers, Marc., Lindsay, Richard., Lauwers, Anne., Henson, Kirklen., Severi, Simone., Pollentier, Ivan. and Keersgieter, An de. 2005. Challenges in scaling of CMOS devices towards 65nm node. Journal of telecommunications and information technology. 1:3-6.

Liang, Xiaoping. and Taur, Y. 2004. A 2-D Analytical Solution for SCEs in DG MOSFETs. IEEE Trans. On Electron Devices. 51:1385-1391.

Lime, Francois., Iniguez, B. and Moldovan, O. 2008. A Quasi-Two dimensional compact Drain-current model for Undoped Symmetric Double-Gate MOSFETs including Short-channel effects. IEEE Trans on Electron Devices. 55:1441-1448.

Lu, Huxin. and Taur, Y. 2006. An analytical potential model for symmetric and asymmetric DG MOSFETs. IEEE Trans on Electron Devices. 53:1161-1168.

Munteanu, Daniela., Autran, Jean-Luc., Loussier, Xavier., Harrison, Samuel., Cerutti, Robin. and Skotnicki, T. 2006. Quantum short-channel compact modeling of drain-current in double-gate MOSFET. Solid-State Electronics. 50:680-686.

Reyboz, M., Rozeau, O., Poiroux, T., Martin, P, and Jomaah, J. 2006. An explicit analytical charge-based model of undoped independent double-gate MOSFET. Solid State Electronics. 50:1276-1282.

Takeuchi, K., Koh, R. and Mogami, T. 2001. A study of the threshold voltage variation for ultra-small bulk and SOI CMOS. IEEE Trans on Electron Devices. 48:1995-2001.

Tsormpatzoglou, Andreas., Dimitriadis, A. Charalabos., Clerc, Raphael., Rafhay, Quentin., Pananakakis, G. and Ghibaudo, Gerard. 2007. Semi-Analytical Modeling of Short-Channel effects in Si and Ge symmetrical Double-Gate MOSFETs. IEEE Trans on Electron Devices. 54:1943-1952.

Tsormpatzoglou , Andreas., Dimitriadis, CA., Clerc, R., Pananakakis, G. and Ghibaudo, G. 2008. Threshold voltage model for short-channel undoped symmetrical double-gate MOSFETs. IEEE Trans on Electron Devices. 55:2512-2516.

Received: May 6, 2009; Revised: July 29, 2009; Accepted: August 4, 2009