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A NOVEL LOW LEAKAGE BODY BIASING TECHNIQUE FORCMOS CIRCUITS

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ABSTRACT

In this paper a body bias technique is proposed for leakage minimization in CMOS VLSI circuits. A gate level body bias controller circuit is designed which dynamically change the threshold voltage of NMOS transistors. When the NMOS transistor is in OFF state, the threshold voltage of transistor is raised by applying reverse body bias through the controller circuit. This reverse body bias raises the threshold voltage of NMOS transistor in the pull down path and hence the sub-threshold leakage current reduces. Here the main focus is to reduce leakage current in NMOS transistors in pull down path because it provides a leakage current path from supply to ground, even in OFF-state. The proposed design is compared with LECTOR technique. Simulation results show that proposed design significantly reduces the power dissipation and gives a low power delay product.

Keywords: Low power, body biasing, sub-threshold leakage, leakage power, threshold voltage.

INTRODUCTION

Modern portable electronic devices such as mobile phones, laptops, PDA's (personal digital assistant)etc are affected by high power consumption which reduces the battery back-up time. The device density of these devices has been increased to improve the performance of the circuit(Wong and Iwai, 2006). So there is a need for low power design methodology to limit the power consumption in high density VLSI chips. Voltage scaling is one of the effective techniques to reduce the power consumption in electronic devices (Haghdad and Anis, 2008). However power saving is obtained at the expense of reduce computational speed (Soeleman *et al*., 2001), increased process and temperature variation (Verma*et al*., 2008). There are basically three sources of power dissipation 1). Dynamic power dissipation due to charging and discharging of current, 2). Short circuit power dissipation, and 3). Static power dissipation. Power dissipation in a logic CMOS circuit (Sayedand Al-Asaad, 2006) can be expressed as,

$$P_{total} = P_{dynamic} + P_{short} + P_{leakage} \quad (1)$$

Dynamic dissipation was the dominating component of total power dissipation in earlier technologies. Now a day's VLSI technology has reached to deep nanometer range so the threshold voltage (V_t) , channel length (L) and gate oxide thickness etc. are need to be scaled drastically (Sinha and Chaudhury, 2013). The scaling of these parameters increases the leakage power dissipation and its contribution increases from 18% at 130nm to 54% at 65nm (Agarwal *et al*., 2004). Moreover, power density is a growing concern in today's high performance chip which even demands for thermal-aware design (Chaudhury *et al*., 2009). The main sources of leakage current (Piguet, 2005) in deep nanometer level are sub-threshold leakage current (I_{SUB}), gate direct tunneling current (I_G), gate induced drain leakage (I_{GIDL}) and reverse bias junction leakage current. Amongst all leakage currents sub-threshold leakage is the dominating component of leakage current. Sub-threshold leakage current is the drain to source current when the transistor is in OFF state which means V_{gs} is less than the V_t. The following equation relates the sub-threshold leakage current (Roy *et al*., 2003).

$$I_{sub\text{-}leakage} = I_0 e^{\frac{V_{gs}-V_t}{\eta V_{th}}}\left(1 - e^{-\frac{V_{ds}}{V_t}}\right) \quad (2)$$

Where, $I_0 = \mu C_{ox}\frac{W}{L}V^2 e^{1.8}$, $V_{th} = \frac{KT}{q}$ and $\eta = 1 + \frac{Cdm}{Cox}$

μ denotes carrier mobility, C_{ox} is the gate oxide capacitance per unit area, *W* and *L* denotes width and length of the channel in MOS transistor, *K* is the Boltzmann constant, *T* is the absolute temperature, q is the electrical charge of conduction, V_{th} is thermal voltage, η denotes the sub threshold ideality factor, C_{dm} is the capacitance of the depletion layer and C_{ox} is the capacitance of the oxide layer (Narendra, 2005).

The primary techniques to reduce the leakage current at circuit level are - transistor stacking, body-biasing and multi-threshold techniques. Multi-Threshold (Mutoh *et*

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al., 1995) (MTCMOS) has emerged as a very popular technique for standby mode leakage power reduction. In this technique, sleep transistors are inserted between the power supply and pull-up network(PUN) (Header) and or between pull down network (PDN) and ground (Footer) to reduce standby leakage current. Dual V_t technique uses the combination of high V_t and low V_t transistors (Wei *et al*., 1999). Low V_t on critical path which is used to maintain the performance, while high V_t transistor assigned to non-critical path which is used to reduce the leakage current. When more than one transistor are connected in series and are in turned OFF state, and then we expect less leakage current to flow. This effect is known as stack effect (Johnson *et al*., 1999). Sleepy stack (Park and Mooney, 2006) technique uses the combination of stacking and sleep transistor insertion in both pull-up and pull-down path. The overall resistance of both the paths reduces because of connecting parallel sleep transistors. The technique operates in a similar manner to the sleep transistor technique, where sleep transistors are turned ON during active mode and turn-OFF during standby mode. Area and propagation delay are the penalty in this technique.

A bootstrap circuit is utilized to raise the input voltage from –VDDto2VDD to suppress the sub-threshold leakage current (Ho *et al*., 2012). LECTOR (Hanchate and Ranganathan, 2004) technique utilizes two leakage control transistors (LCT) which are inserted between PUN and PDN in each CMOS gate as shown in Figure 1. Leakage control transistors causes increase in the resistance of the path from V_{dd} to ground, since one of the LCT's always near its cut-OFF region, therefore decreasing the leakage current. This technique is good for leakage reduction but this technique is not capable of reducing propagation delay.

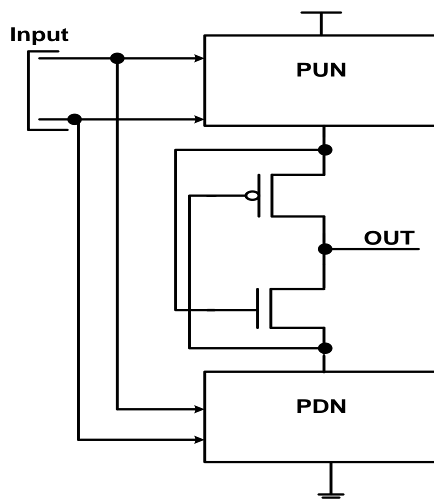

Fig. 1. LECTOR CMOS design.

Proposed Design

The V_t is one of the most important design parameters for reducing the leakage power in CMOS circuit. The V_t can be controlled in many different ways (Sumita *et al*., 2005; Hirano *et al*., 2008) - one way is to control the source to bulk voltage. Sub-threshold leakage current in NMOS transistor can be reduced by overdriving the NMOS transistor (Ananthan *et al*., 2004) as shown in Figure 2(a). In this way V_t of transistor will increase. The proposed technique is based on gate level body-biasing scheme as shown in Figure 2(b). The PDN body voltage (V_bulk) is generated dynamically by the built in body bias controller circuit which is based on output node voltage. When the output voltage is 1V, NMOS transistor in the body bias controller circuit transfers a reverse body-bias voltage Va= Vss–ΔV to the bulk (body) of NMOS transistor in PDN which is in OFF-state. Reverse body-bias raises the V_t of NMOS transistors and hence the sub-threshold leakage current reduces. In this way, the overall leakage power is suppressed because NMOS transistor (Kimand Roy, 2002) conducts maximum amount of sub-threshold leakage current from supply (V_{dd}) to ground. On the other hand if output voltage is 0V, PMOS transistor in body bias controller circuit transfers no body-bias (0V) to the body of NMOS transistor in PDN. The leakage current from V_{dd} may or may not find the leakage path to ground depending upon the input vectors. Moreover, there is a need to change the V_t gradually to suppress leakage because any drastic increase of reverse bias to the source-bulk of NMOS transistor will lead to increase tunneling which may consequently damage the transistor (Rabaey *et al*., 2003). So it is important to control the bulk voltage of transistor appropriately. To minimize the capacitive effect at the output node of logic gate and the circuit, the body bias controller circuit can be downsized.

Simulated DC characteristic of three input conventional, LECTOR and proposed design using 3-input N and gate is shown in Figure 3. This characteristic is simulated, when input B and C is fixed to 1V and A is varied from 0 to 1V.

Simulated DC characteristic of three input conventional, LECTOR and proposed design using 3-input N and gate is shown in Figure 3. This characteristic is simulated, when input B and C is fixed to 1V and A is varied from 0 to 1V. We can observe that, the output current is high in proposed design because of which DC characteristic shifts towards right. This high current is due to additional transistors added at the output node by the body-bias controller. Additional transistor causes more capacitive load (C_L) at the output node. Compared to conventional and LECTOR design, more dynamic power (Kang and Leblebici, 2003) can be expected, if we see the equation of dynamic power as given in Eq. (3).

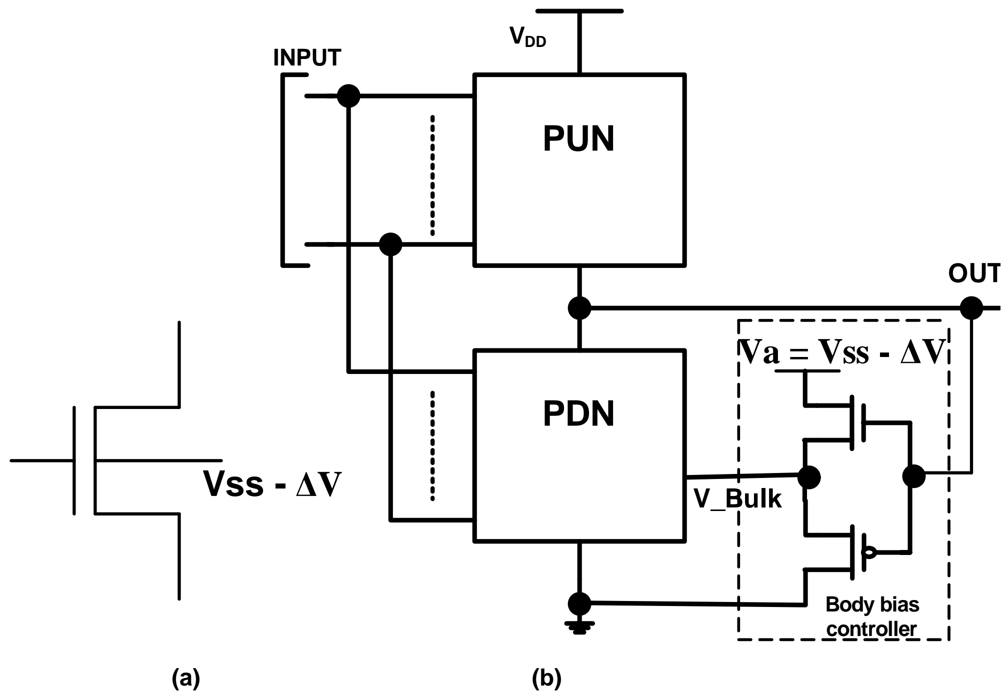

Fig. 2 .(a) NMOS transistor in idle mode (b) Proposed Design.

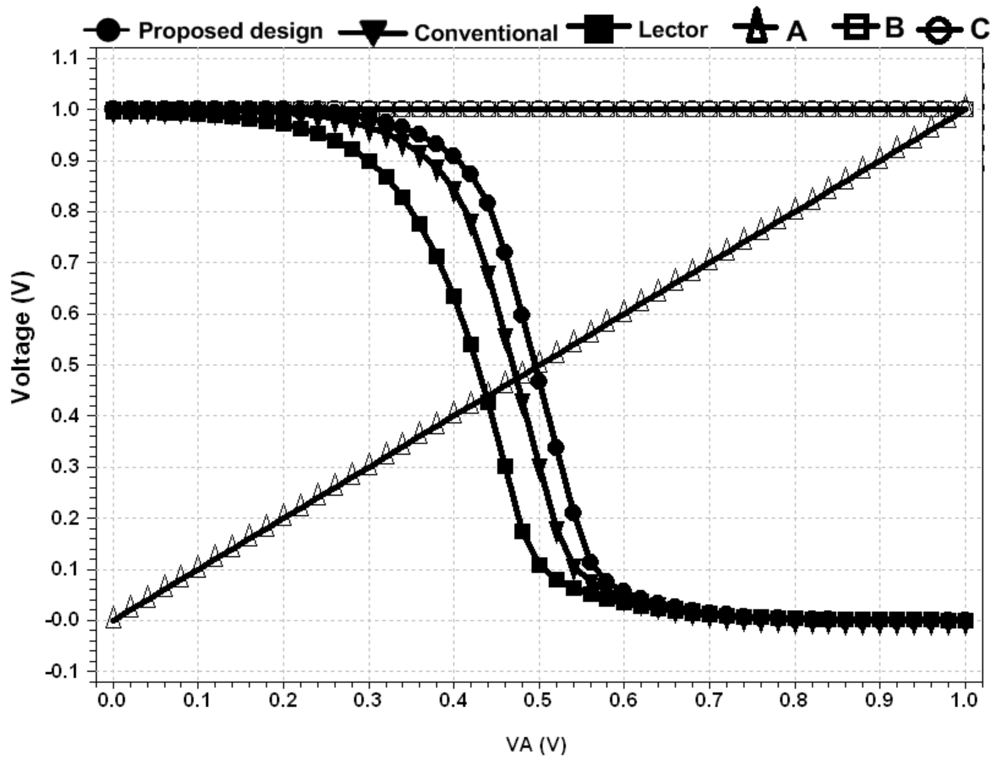

Fig. 3. Simulated DC characteristic of 3-input NAND gate.

$$P = C_L V_{dd}^2 f_{op} \quad (3)$$

Where C_L is the load capacitance, V_{dd} is the supply voltage and *fop* is the frequency of operation.
In CMOS digital circuits, propagation delay of a gate (Park and Mooney, 2006) is approximately given by

$$t_{pd} \,\alpha\, \frac{C_L V_{dd}}{I_{DS}} = \frac{C_L V_{dd}}{A(V_{dd} - V_t)^2} \quad (4)$$

Where C_L is the load capacitance, V_{dd} is the supply voltage, I_{DS} is the drain current in the saturation, V_t is the threshold voltage and A is constant. From the expression of propagation delay we can expect that as we increase the load capacitance delay time (t_{pd}) will increase, again with a high drain current (I_{DS}) delay will be small. In the proposed design, we have a higher output node capacitance so we expect delay to rise but this is nullified by the increase in drain current because of additional capacitive load, which we have observed in DC characteristic. So the proposed approach has the least propagation delay.

Leakage current in nano-scale MOSFET devices is mainly guided by sub-threshold leakage current. When a transistor is OFF, it means $V_{gs}$is less than V_t, so the transistor is in weak inversion. The sub-threshold current is generally expressed as Eq. (2). Sub-threshold current also vary exponentially with V_t (Kao and Chandrakasan, 2000) and can be given as

$$I_{leakage} = \frac{W}{W_0} I_0 e^{(V_{gs} - V_t)/\eta V_{th}} = \frac{W}{W_0} I_0 10^{(V_{gs} - V_t)/S} \quad (5)$$

Where V_{th} is thermal voltage, W is width, n is a constant and S= nV_{th}ln10 is the sub-threshold slope of 100mV/decade. For each 100mV decrease in V_t will cause an order of magnitude increase in leakage current.
LECTOR technique minimizes the leakage current by inserting leakage control transistors (LCT) between PUN and PDN. This LCT provides stack effect. In LECTOR technique, one of the two LCT is always near cut-OFF, because of which leakage suppression is not high enough. In proposed design, we have implemented a body-bias control scheme to provide reverse body bias to all the OFF transistors in pull-down path. The OFF transistors in pull-down path raise the V_t and hence we expect more leakage suppression. This fact can be easily understood by sub threshold current expression as in Eq.(2). As we increase V_t by reverse body bias, the difference (V_{gs} - V_t) over the exponential term get reduced. Consequently the sub-threshold leakage current will also reduce. In the proposed design we are using the concept of body–biasing technique which provides maximum resistance to leakage path, through the NMOS transistors in PDN when these are in OFF state. In ON state, as there is no bias so no change in path resistance, as a result propagation delay of proposed design is minimum.

Transient characteristics of three inputs NAND gate for conventional, LECTOR and proposed design are shown in Figure 4, from which we can observe that the proposed design is operating at a correct output voltage level.

RESULTS AND DISCUSSION

In this section, the proposed design is compared with LECTOR and conventional logic gates in terms of average power dissipation and delay. To analyze the performance parameter we have used Tanner EDA tool using 65nm PTM (predictive technology model) technology with a power supply of 1V.

Average power dissipation is calculated by asserting the semi-random input vectors. Large numbers of input vectors are included in the combination. Table 1 shows average power dissipation of different CMOS gates and circuits. We can observe that, as the reverse body-bias voltage V a gradually increases, more power reduction is achieved. This reverse body-bias voltage can be increased up to a certain limit after that tunneling will start which may damage the transistor. The maximum power saving is achieved in NAND gate because with CMOS implementation PDN forms stack with series connected NMOS transistors, which significantly reduces power dissipation. In case of NOR gate leakage power reduction is achieved however, at relatively higher reverse body bias. This is because NMOS transistors in the pull-down path of a NOR gate are in parallel which reduces the path resistance. The arrangement of NMOS transistors in CMOS implementation of full-adder circuit are in series as well as in parallel, so leakage reduction is achieved at moderate voltage level of reverse body-bias.

Power dissipation is a strong function of temperature, as the temperature increases power dissipation increases. This happens because leakage current depends on thermal equivalent voltage (Haghdad and Anis, 2008). The effect of power dissipation on temperature for NAND3 gate is shown in Figure 5. It can be observed from the Figure 5 that as reverse body bias voltage increases, better power reduction is achieved in proposed design compared to conventional and LECTOR technique.

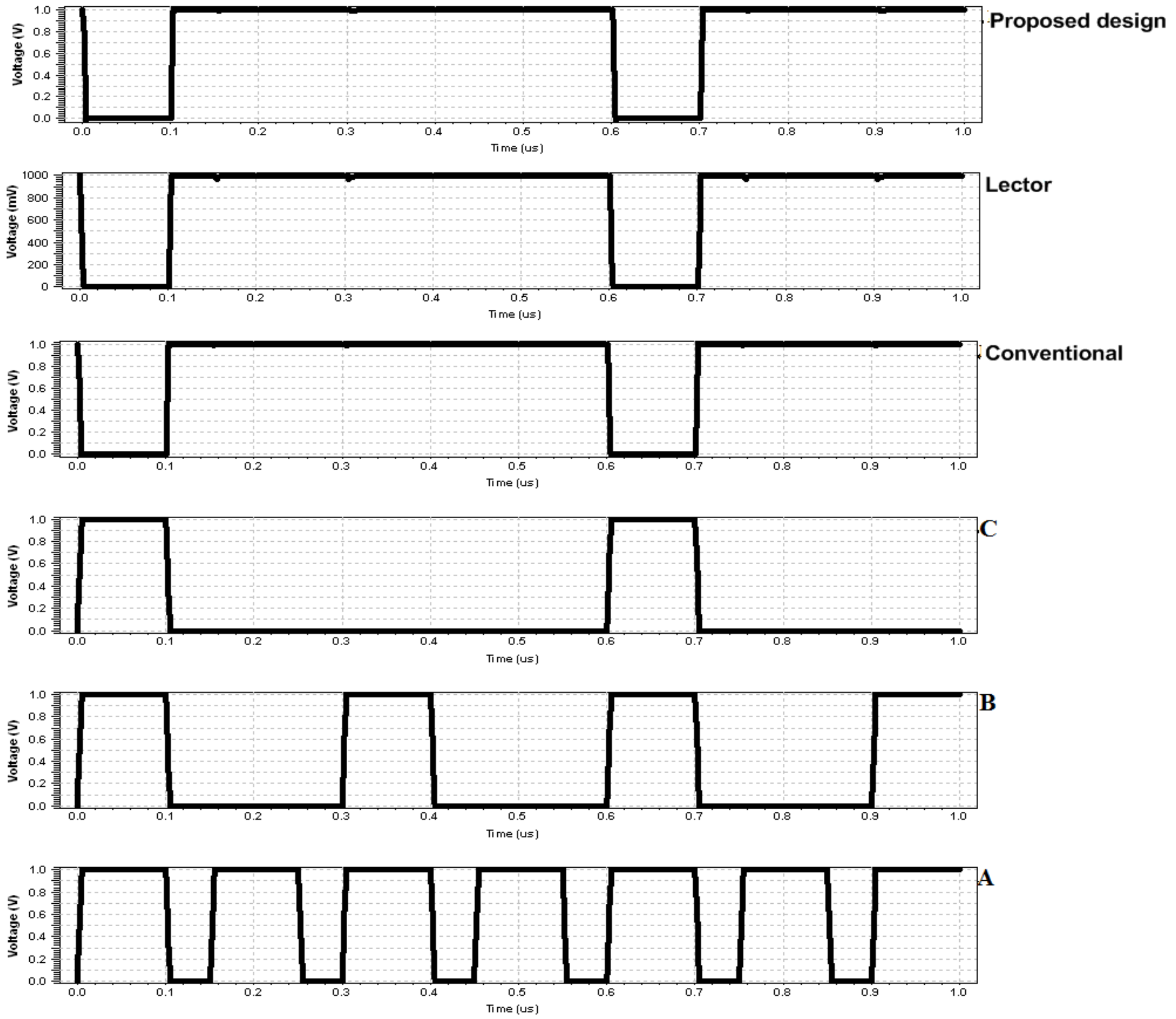

Fig. 4. Transient characteristic of 3-input NAND gate.

Table 1. Average power (W) on CMOS gates and circuits at 65nm process technology.

	Nand3	% saving	NOR3	% saving	Full Adder	% saving
Conventional	2.35E-07	----------	5.52E-07	-----------	9.94E-06	----------
LECTOR	1.77E-07	24.7	4.69E-07	14.2	8.40E-06	15.4
Proposed design at	-------------	----------------	--------------	-------------	-----------	---------
Va= -0.1V	1.55E-07	34	5.42E-07	1.8	8.72E-06	12.2
Va= -0.22V	1.52E-07	35.3	4.85E-07	12.1	8.32E-06	16.2
Va= -0.27V	1.44E-07	38.7	4.67E-07	15.39	8.17E-06	17.8
Va= -0.32V	1.38E-07	41.3	4.62E-07	16.3	8.12E-06	18.3
Va= -0.36V	1.33E-07	43.4	4.58E-07	17.02	7.16E-06	27.9

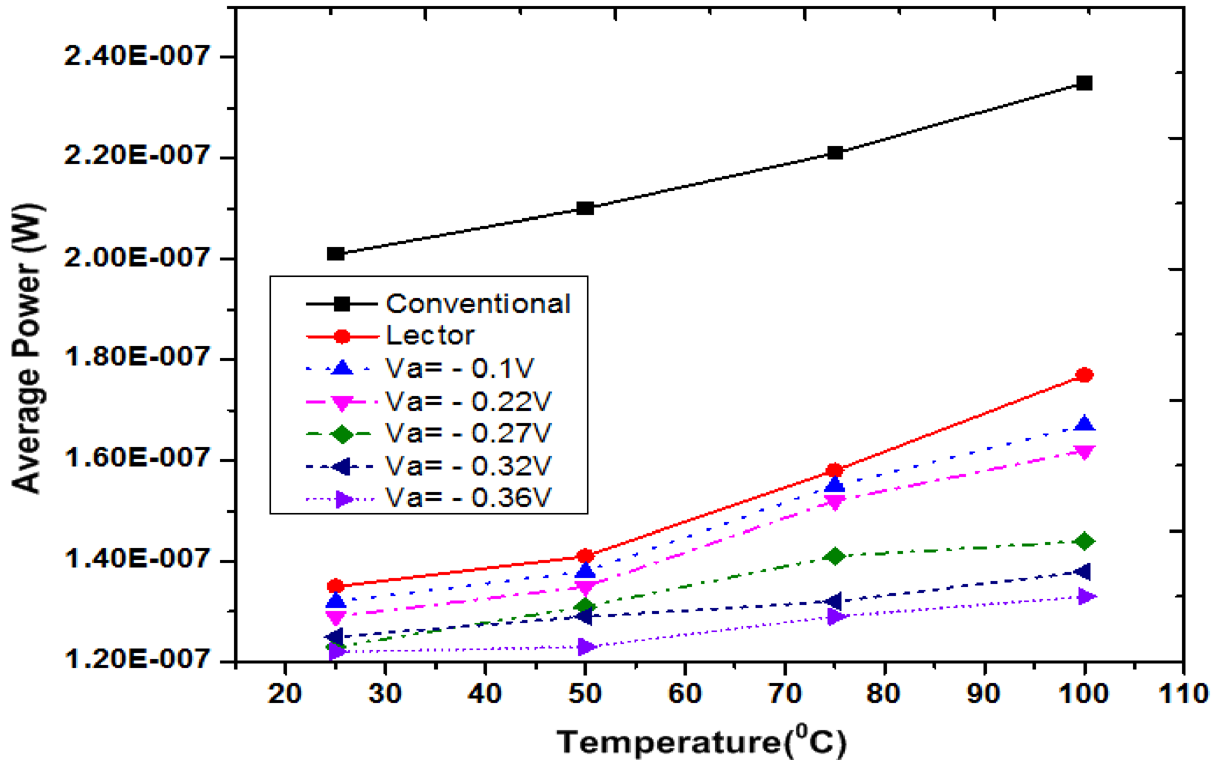

Fig. 5. Temperature variation versus average power of NAND3 gate.

Table 2 shows comparative analysis of propagation delay of conventional, LECTOR and proposed design at different reverse body-bias voltages. In LECTOR technique, extra LCT are inserted to reduce the leakage power but these extra transistors raises the propagation delay of the circuit (Venkatachalam and Franz, 2005). The proposed design significantly reduces the propagation delay over LECTOR technique because LCT are not inserted between PUN and PDN.
However, propagation delay in the proposed design is higher than the conventional design because V_t in the proposed design is adjusted to have a higher value. We can observe from the Table 2 that NAND gate has a low propagation compared to NOR gate. This is because the arrangements of PMOS transistors in pull-up circuitry in NAND gate are in parallel which means less resistance in the pull-up path and hence the propagation delay is less. Delays are also measured for all the three designs (implemented to NAND3) at different temperatures and are shown in Figure 6. As the temperature increases delay of the circuit also increases. However, proposed design has lesser delay penalty than the LECTOR technique.

Table 2. Propagation delay(s) on CMOS gates and circuits at 65nm process Technology.

	Nand3	**% Penalty**	**NOR3**	**% Penalty**	**Full Adder**	**% Penalty**
Conventional	4.11E-11	----------	7.68E-11	-----------	9.20E-10	----------
LECTOR	3.52E-10	88.32	3.91E-10	80.35	1.61E-09	42.85
Proposed design at	---------------	--------------	--------------	------------	-------------	--------------
Va= -0.1V	1.09E-10	62.29	2.40E-10	68	9.87E-10	6.7
Va= -0.22V	2.08E-10	67.89	2.43E-10	68.39	1.01E-09	8.91
Va= -0.27V	1.05E-10	71.84	2.44E-10	68.52	1.19E-09	22.68
Va= -0.32V	1.98E-10	79.24	2.59E-10	70.34	1.24E-09	25.8
Va= -0.36V	2.35E-10	82.51	2.99E-10	74.34	1.37E-09	32.84

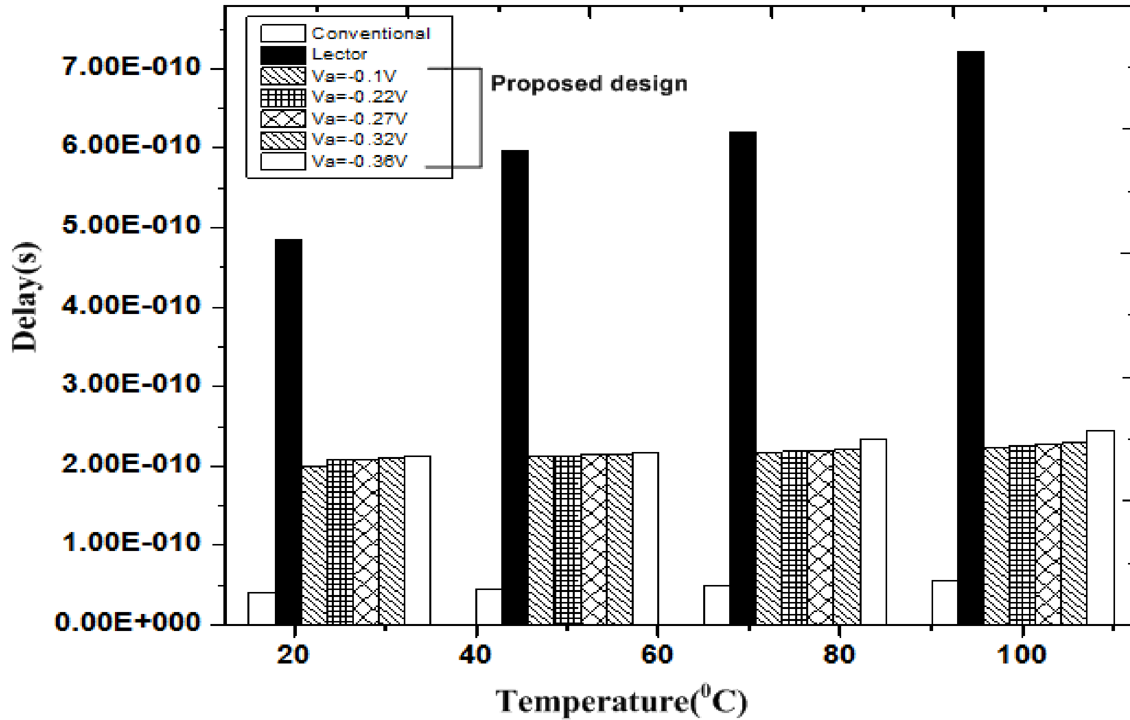

Fig. 6. Temperature variation versus delay of NAND3 gate.

Table 3 presents power-delay product (PDP) of CMOS NAND and NOR gates and Full Adder circuits. It can be observed that the proposed design has a low PDP than LECTOR and conventional technique. The (+) and(-) sign indicates that power delay product is either increasing or decreasing with respect to conventional circuit. Moreover, power delay product of proposed design is better than conventional design.

Table 3. Power-delay product (J) on CMOS gates and circuits at 65nm process Technology.

	Nand3	% Variation	NOR3	% Variation	Full Adder	% saving
Conventional	9.65E-18	----------	4.24E-17	-----------	9.14E-15	----------
LECTOR	1.90E-16	+94.92	1.83E-16	+76	1.35E-14	+32.2
Proposed design at						
Va= - 0.1V	1.69E-17	+42.89	1.30E-16	+67.4	8.61E-15	-10.7
Va= - 0.22V	3.16E-17	+69.46	1.17E-16	+63.7	8.38E-15	-8.3
Va= - 0.27V	1.51E-17	+36.09	1.14E-16	+62.8	9.70E-15	+5.7
Va= - 0.32V	2.73E-17	+64.65	1.20E-16	+64.5	1.01E-14	+9.5
Va= - 0.36V	3.13E-17	+69.16	1.37E-16	+69.003	9.81E-15	+7.33

CONCLUSION

In this paper we have pointed out the problem associated with LECTOR technique. We then propose a body bias technique for low leakage and high speed. Simulation based on 65nm process technology shows that the proposed technique is capable of reducing leakage power dissipation and minimizing the delay efficiently which leads to a lower power delay product.

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